What is claimed is:

1. A method for fabricating a semiconductor device which is formed on a semiconductor substrate and which operates as a bipolar transistor provided with an emitter, a base, and a collector, said method comprising:

a step (a) of forming said collector of a first conductivity type at a portion of a surface of said semiconductor substrate,

a step (b) of forming a first insulating layer on said semiconductor substrate and subsequently forming, in a portion of said first insulating layer situated above said collector, a collector opening portion reaching said collector,

a step (c) of epitaxially growing, on said semiconductor substrate, a semiconductor layer including at least a layer of a second conductivity type constituting said base,

a step (d) of forming, on said semiconductor substrate, an etching stopper layer which serves as an etching stopper against dry etching and which has insulating ability and a masking layer against wet etching in such a way that said masking layer overlies said etching stopper layer,

a step (e) of exposing a part of said etching stopper layer by removing a part of said masking layer by means of dry etching,

a step (f) of forming a base junction opening portion reaching said semiconductor layer by subjecting said part of said etching stopper layer exposed by means of said dry etching of said step (e) to a wet etching treatment using the remaining part of said masking layer as a mask,

a step (g) of layering, on said semiconductor substrate, a first conductor layer and a second insulating layer and subsequently forming a base opening

portion reaching said etching stopper layer by carrying out a dry etching treatment so that said masking layer, said first conductor layer, and said second insulating layer are penetrated locally,

a step (h) of forming a third insulating layer covering a side surface exposed to said base opening portion,

a step (i) of exposing said semiconductor layer at the bottom of said base opening portion by removing a portion of said etching stopper layer exposed to said base opening portion by means of a wet etching treatment, and

a step (j) of forming said emitter by filling up said base opening portion.

2. The semiconductor device fabrication method as claimed in claim 1 wherein:

said masking layer is formed by an electrical conductor.

3. The semiconductor device fabrication method as claimed in claim 1 wherein:

in said step (c), as said semiconductor layer, a heterojunction semiconductor layer serving as said layer of the second conductivity type which is heterojunctioned to said collector, and an undoped emitter semiconductor layer which is heterojunctioned to said heterojunction semiconductor layer are formed, in that order, on said semiconductor substrate in said collector opening portion by epitaxial growth, and

in said step (j), a second conductor layer doped with impurities of said first conductivity type is formed in said base opening portion, whereby said first conductivity type impurities are diffused into said emitter semiconductor layer from said second conductor layer.

4. The semiconductor device fabrication method as claimed in claim 3 wherein:

said heterojunction semiconductor layer comprises at least one of SiGe, SiGeC, and SiC.

5. The semiconductor device fabrication method as claimed in claim 1 wherein:

in said step (b), a reducing film including a material selected from among polysilicon, amorphous silicon, and silicon nitride is formed on said first insulating layer, and said collector opening portion is formed through portions of said reducing film and said first insulating layer situated above said collector.

6. The semiconductor device fabrication method as claimed in claim 1 wherein:

in said step (g), a junction leak prevention layer is formed below a surface of said semiconductor layer exposed to said base junction opening portion by introducing impurities of said second conductivity type by means of an ion implantation treatment using said remaining masking layer as a mask, and said first conductor layer and said second insulating layer are layered on said semiconductor substrate.

7. A semiconductor device which is formed on a semiconductor substrate and which operates as a bipolar transistor, said semiconductor device comprising:

a collector of a first conductivity type formed at a portion of a surface of said semiconductor substrate,

a first insulating layer so formed on said semiconductor substrate as to have, in a portion thereof situated above said collector, a collector opening portion,

a semiconductor layer which is grown epitaxially on said semiconductor substrate and said first insulating layer in said collector opening portion and which includes at least a layer of a second conductivity type for constituting a base,

an etching stopper layer which serves as an etching stopper against dry etching and which has insulating ability, and a masking layer against wet etching, said etching stopper layer and said masking layer being so layered sequentially above a predetermined portion of said semiconductor layer as to have a base junction opening portion,

a first conductor layer covering said semiconductor layer and said masking layer in said base junction opening portion,

a second insulating layer formed on a predetermined portion of said first conductor layer,

a base opening portion so formed as to pass completely through said etching stopper layer, said masking layer, said first conductor layer, and said second insulating layer,

a third insulating layer covering side surfaces of said masking layer, said first conductor layer, and said second insulating layer exposed to said base opening portion, and

an emitter connected to a second conductor layer filling up said base opening portion.

8. The semiconductor device fabrication method as claimed in claim 2 wherein:

said base comprises an intrinsic base and an extrinsic base,

said intrinsic base comprises a central portion of said semiconductor layer, and

said extrinsic base comprises said masking layer and a portion of said semiconductor layer other than said central portion.

9. The semiconductor device fabrication method as claimed in claim 8 wherein:

said masking layer comprises polysilicon.

10. The semiconductor device as claimed in claim 7 wherein:

said masking layer comprises a conductor,

said base comprises an intrinsic base and an extrinsic base,

said intrinsic base comprises a central portion of said semiconductor layer, and

said extrinsic base comprises said masking layer and a portion of said semiconductor layer other than said central portion.

11. The semiconductor device as claimed in claim 10 wherein:

said masking layer comprises polysilicon.